Name of Teaching Staff	:	Dr. (Mrs.) Poonam A. Kadam
Designation	:	Assistant Professor
Department	:	Electronics & Telecommunication Engineering
Date of Joining the Institution	:	3.2.2006
Email ID	:	poonam.kadam@djsce.ac.in
Office Contact	:	022-42335000 (Ext.1227)
Google Scholar Link	:	https://scholar.google.com/citations?user=LbBPwTE AAAAJ&hl=en
Researchgate Link:	:	https://www.researchgate.net/profile/Poonam-Kadam
ORCID	:	https://orcid.org/my-orcid?orcid=0000-0003-3635-7872
Qualifications with Class / Grade	:	1. Ph.D. in Technology (Electronics & Telecommunication Engineering) from University of Mumbai on Topic "Design and Analysis of Broadband and Multiband Antennas using Defected Ground Plane Structure". 2. M.Tech. in Electronics Engineering from I.I.T. BHU, 2003, 1st class with Distinction 9.13 CGPA. 3. B.E. (Electronics Engineering) from SGGS Institute of Technology, SRTMU, 2001, 76.30%, 1st class.
Total Experience in Years	:	**Teaching**: **19 years** 1. Assistant Professor, Electronics & Telecommunication Engg. Department, D. J. Sanghvi College of Engineering from 2.7.2007 to till date. 2. Lecturer (Adhoc), IT Department, D. J. Sanghvi College of Engineering from 3.2.2006 to 30.06.2006 and from 11.7.2006 to 01.7.2007. 3. Lecturer, Electronics Department, SGGS Institute of Technology, from 3.2.2003 to 2.2.2006.
Papers Published in Journal:	:	**International**: **7** [1] P. A. Kadam and A. A. Deshmukh, "Multiband microstrip antenna using modified pi-shape slot on ground plane", International Journal of Wireless and Microwave Technologies, vol.9, no.1, pp. 23-35, 2019. [2] P. A. Kadam and A. A. Deshmukh, "Modified ground plane multiband rectangular Microstrip antenna with reduced cross-polar radiation", Progress in Electromagnetics Research C, vol. 100, 59-71, 2020. [3] P. A. Kadam and A. A. Deshmukh, "Compact wideband microstrip antenna with modified ground plane", International Journal of Microwave and Optical Technology, vol. 15, no. 3, pp. 228 – 237, May 2020.

Papers Presented in Conferences	:	[4] A. A. Deshmukh, P. Kamble and P. A. Kadam," Design of slots cut rectangular microstrip antenna backed by modified ground plane for wider bandwidth", International Journal Microwave and Optical Technology, pp. 228-237, vol. 15, No. 3, Nov. 2020. [5] P. A. Kadam and A. A. Deshmukh, "Rectangular microstrip antennas backed by modified ground plane for reduced cross polar radiation", International Journal Microwave and Optical Technology, vol. 16, No. 1, January 2021. [6] P. A. Kadam and A. A. Deshmukh, "Regular shape microstrip antennas backed by bow-tie shape ground plane for enhanced antenna characteristics" International Journal of Electronics and Communications (AEU), May 2021. [7] P. A. Kadam and A. A. Deshmukh "Gap-coupled microstrip antennas backed by rectangular slot cuts ground plane", International Journal of RF and Microwave Computer-Aided Engineering, Aug. 2021. **National**: **3** [1] Poonam Varma, V. Shahane, "Efficient VLSI computing paradigm using a Novel 5*5 Universal Reversible gate", DJSCOE & NMIMS – National conference on information and communication Technology New Horizon in Technology and Applications, PP.4, March 01-03, 2007. [2] Poonam Kadam, Akshita J, Bhavin M, Ronak H, "Multiplier design using SCRL technique" – NCCT 2011. [3] Poonam A. Kadam, Amit A. Deshmukh, et al., "Analysis and Resonant length formulation of Dual-Band Microstrip antenna with Modified ground", National Conference on Communications NCC 2019. **International**: **29** [1] Amit Deshmukh, Adil Parvez, Priyanka Verma, Ami Desai, Poonam Kadam and Kamala Prasan Ray, "Space Fed Ring Microstrip Antenna array with Stacked Rectangular Microstrip Antenna Feed", INDICON 2016. [2] Poonam Kadam, Kapil Gavali, "VLSI design of high speed Vedic multiplier for FPGA implementation", in 2016 IEEE conference on Engineering and Technology ICETECH 2016, 17th and 18th March 2016. [3] Kapil Ram Gavali, Poonam Kadam: High Throughput Architecture of DCTQ Processor suitable for FPGA Implementation, in 2016 IEEE International Conference on Communication Systems and Networks, COMNET 2016, India. [4] Poonam Kadam, Amruta Oza, "Techniques for Sub-Threshold Leakage Reduction in Low Power CMOS Circuit Designs, International Journal of Computer Applications (0975 – 8887) Volume 97– No.15, July 2014. [5] Poonam Kadam, Amruta Ozam "Low Power High Speed Multiplier Design based on MTCMOS Technique, Communication on Applied

Electronics, ISSN: 2394-4714 Foundation of Computer Science FCS, New York, USA Volume 5 – No.7, July 2016.

[6] Poonam Kadam, Sahil Thapar et al., "Comparative Analysis of Routing Protocols", International Journal of Computer Application, 2014.

[7] Poonam Kadam, Bhakti Patel "Comparative Analysis of Adiabatic logic techniques", International Journal of Computer Application, (0975-8887), ICCT 2015.

[8] Poonam Kadam and Bhakti Patel, "Modified PFAL adiabatic technique for Low Power", Communication on Applied Electronics, Dec. 2015.

[9] Poonam Kadam, Nilima Parmar, "Combined Architecture for AES Encryption and Decryption using FPGA", Communication on Applied Electronics- ISSN: 2394- 4714, ICCT 2015.

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[15] A. A. Deshmukh, Shafin Nagarbowdi, P. A. Kadam, A.A. Odhekar, "Broadband Gap-coupled Isosceles Triangular Microstrip Antennas, International Conference on Emerging Trends & Innovation in ICT (ICEI) Pune Institute of Computer Technology, Pune, India, Feb 3-5, 2017.

[16] A. A. Deshmukh, P. A. Kadam, Shefali Pawar, K P Ray, "Analysis of Single Shorted Square Microstrip Antenna", International Conference on Emerging Trends & Innovation in ICT (ICEI) Pune Institute of Computer Technology, Pune, India, Feb 3-5, 2017.

[17] A. A. Deshmukh, P. A. Kadam , Darshan Gala, K P Ray, "Multi-band Square Microstrip Antenna Using Defected Ground Plane", IEEE, ICCUBEA2017.

[18] Amit A. Deshmukh, Poonam Kadam, Akshay Doshi, Darshan Gala, "Wide band Designs of Rectangular Microstrip Antenna Using modified ground plane", IEEE, ICAC2017.

[19] Poonam A. Kadam, Amit A. Deshmukh et al., "Design and Analysis of Multiband defected ground plane MSA", International Conference on Communication, Information and Computing Technology, IEEE, 2018 at SPIT.

[20] Amit A. Deshmukh, Poonam A. Kadam, et al., "Air Suspended Multiband E-shaped Antenna", International Conference On Computing, Communication, Control and Automation, IEEE, 2018, Pune.

[21] Amit A. Deshmukh, Poonam A. Kadam, et al., "Multi-Resonant Wide Band Rectangular Microstrip Antenna with U-Shape and Rectangular Slots", International Conference on Wireless Communication, Springer, 2017.

[22] Amit A. Deshmukh, Poonam A. Kadam, et al., "On the Design of Circularly Polarized U-slot cut square Microstrip Antenna", IEEE 2017 International conference on Communication systems & IT Applications, April 2017.

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[24] Jeet Sanghavi, Alay Shah, Saurabh Rane, Naitik Shah, Siddharth Nayak, Poonam Kadam, "Agricultural Productivity Enhancement System & Livestock Management using Internet of Things", International Conference on Advances in Electronics, Computer & Communication, 2018.

[25] Poonam A. Kadam, Amit A. Deshmukh, et al., "Improved Compact Broadband Defected Ground Microstrip Antenna", International Conference in Computing, Communication and Control, IEEE 2019.

[26] Poonam A. Kadam, Amit A. Deshmukh, "Analysis of Compact Dual Band Defected Ground Microstrip Antenna for WLAN Application", International Conference on Wireless Communication, Springer, 2019.

[27] Anuja Odhekar, Amit Deshmukh, Poonam Kadam and Sanjay Deshmukh, "Novel Design of Square Microstrip Antenna with Circular Slots for Circular Polarization", 2018 15th IEEE India Council International Conference (INDICON), 2018.

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[29] Poonam A. Kadam, Amit A. Deshmukh, "Gap-Coupled Microstrip Antenna Backed by Rectangular Slots Cut Ground Plane for Enhanced

		Bandwidth", International Conference on Wireless Communication ICWiCOM, 2021.	
Area of Specialization	:	**Antennas and Microwave, VLSI Design**	
PhDs / Projects Guided	:	**Projects at Masters level:**	05
Books Published / IPRs / Patents	:	1. Basic VLSI Design 2. Advanced VLSI Design 3. IC Technology 4. VLSI Design and Technology	Tech Knowledge Publication
Professional Memberships	:	Life Member of Indian Society for Technical Education (ISTE)	LM 57594
Awards	:	Best paper Award	"Air Suspended Multiband E- shaped Antenna", International Conference On Computing, Communication, Control and Automation, IEEE, 2018, Pune "VLSI Design of High Speed Vedic Multiplier for FPGA Implementation" International conference on Engg. & Technology ICETECH 2016, Tamilnadu
			"Efficient data path Designing Using Reversible Conservative Logic" on 8th WSEAS International conference on Circuits and System, 2004.
Grants fetched	:	Project Research Grant	University of Mumbai, 2016
Interaction with Professional Institutions	:	Reviewer	➢ IETE Journal of Research ➢ IEEE Transactions on Antennas and Propagation ➢ Progress in Electromagnetic Research (PIER Journal)
Subjects Taught	:	**UG Level:** ➢ Digital System Design ➢ VLSI Design ➢ Computer Communication Network ➢ Control System ➢ Digital Communication **PG Level:** ➢ CMOS Mixed signal VLSI	

Projects Guided	:	**UG Level:**	
		1. Implementation of Smart Oscilloscope using Android Platform (AY 2015-2016) 2. Implementation of a system to access nearest hospital during emergencies using GPs and GSM (AY 2016-2017) 3. Hazardous gas emission monitoring system with centralized server (AY 2016-2017) 4. Increasing agricultural productivity using IoT and livestock management (AY 2017-2018) 5. Design of an energy efficient arithmetic circuit using reversible logic (AY 2017-2018) 6. Light fidelity based data transmission (AY 2018-2019) 7. Room service robot with security features using Image processing (AY 2018-2019) 8. Industrial Liquid Mixing Automation Using PLC and Microcontroller. (AY 2019-2020) 9. SnapRV32 – A 32-bit processor (AY 2019-2020) 10. Floating Point Single Precision ALU using Verilog (AY 2020-2021) 11. Universal Asynchronous Receiver Transmitter (AY 2020-2021)	
		PG Level: 1. Performance Analysis of Energy Efficient Adiabatic Technique for Low Power VLSI Design (AY2014-16) 2. Design & Implementation of high speed low power VLSI circuit (AY2015-16) 3. Low Power Multiplier Design Using Adiabatic Logic (AY2012-13) 4. FPGA Implementation of High Performance VLSI Architecture for AES Algorithm (AY2014-16) 5. Efficient VLSI Design of DCTQ Processor (AY2014-16)	
Recommended Students for Higher Education	:	**Name of the Student** Shreya Gupta Rani Saklecha Prachi Sadarangani Dhoot Ayush Sanghavi Jeet Keval Prakash Kamdar Shah Avi Madhura Daptardar Chirag Mulchandani Rhythm Patwa Yash Jain	**University/Industry** Purdue University NYU Tandon Northeastern University Arizona State University University of Maryland Georgia Institute of Technology University of Southern California Rutgers University Columbia University, New York University of North Carolina at Charlotte Columbia University, New York
Institute/Department Responsibility handled:	:	➢ Time table Coordinator ➢ NAAC Criteria 5 Department Level Coordinator ➢ NBA Criterion 8 Department Level Coordinator ➢ Admission Committee Member ➢ Alumni Coordinator	